(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 333 132 A2**

(12) # EUROPEAN PATENT APPLICATION

(21) Application number: **89104509.8**

(51) Int. Cl.[4]: **H01L 23/50**

(22) Date of filing: **14.03.89**

(30) Priority: **15.03.88 JP 62552/88**

(43) Date of publication of application:
20.09.89 Bulletin 89/38

(84) Designated Contracting States:
DE FR GB

(71) Applicant: **NEC CORPORATION**
33-1, Shiba 5-chome, Minato-ku
Tokyo 108(JP)

(72) Inventor: **Sakamoto, Mitsuru,**
c/o NEC Corporation 33-1, Shiba 5-chome
Minato-ku Tokyo(JP)
Inventor: **Hamano, Kuniyuki**
c/o NEC Corporation 33-1, Shiba 5-chome
Minato-ku Tokyo(JP)

(74) Representative: **Glawe, Delfs, Moll & Partner**
Patentanwälte
Postfach 26 01 62 Liebherrstrasse 20
D-8000 München 26(DE)

(54) **Semiconductor device having multilayered wiring structure with a small parasitic capacitance.**

(57) The semiconductor device of the present invention includes a semiconductor substrate on which are formed semiconductor elements, and a plurality of wiring layers formed on the semiconductor substrate via porous insulating films. The surface of the plurality of the wiring layers is preferably covered with a compact insulating film. The size of the pores in the porous insulating film is preferably 5 nm to 50 nm in diameter, and the volume of the pores in the porous insulating film is preferably 50% to 80% of the total volume of the porous insulating film. The porous insulating film is formed by subjecting a mixed insulating film of a basic oxide and an acidic oxide to a heat treatment to precipitate only either one of the basic oxide and the acidic oxide, and then dissolving out selectively the basic or acidic oxide precipitated.

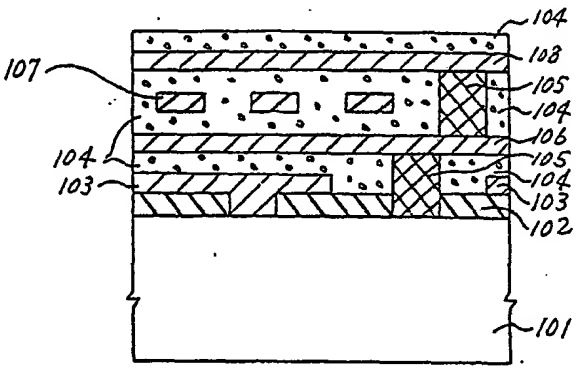

Fig. 1

EP 0 333 132 A2

SEMICONDUCTOR DEVICE HAVING MULTILAYERED WIRING STRUCTURE WITH A SMALL PARASITIC CAPACITANCE

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a wiring structure for a semiconductor device, and more particularly to a semiconductor device having a multilayered wiring structure with a small parasitic capacitance.

Description of the Related Art

With the view toward establishing a larger scale of integration for semiconductor devices, there are strong demands for development of techniques for making the wiring width and wiring spacing more minute and for multilayering of wirings. Under these circumstances, reduction in the parasitic capacitance of wirings becomes important in the wiring technique together with reduction in the wiring resistance. The reason for this is that the parasitic capacitance increases with the increase in the wiring density or with multilayering of the wirings so that it becomes difficult to diminish the power consumption during dynamic operation of semiconductor elements. Furthermore, the reduction in the parasitic capacitance of wirings brings about an improvement in the speed of signal transmission between semiconductor elements which is effective in increasing the operational speed of semiconductor devices.

In order to reduce the parasitic capacitance, it becomes necessary to reduce the relative dielectric constant of the interlayer insulating film between the multilayered wirings. As such interlayer insulating films, there have been known inorganic insulating films like silicon oxide film as disclosed in "Proceedings of Third International IEEE VLSI Multilevel Interconnection Conference," 1986, pp. 100-106 or in "Proceedings of First International IEEE VLSI Multilevel Interconnection Conference," 1984, pp. 37 - 44, organic insulating films like polyimide as disclosed in IEEE Journal of Solid-State Circuits, Vol. SC-13, No. 4, 1978, pp. 462-467, and the like. However, since the relative dielectric constant ϵ of the former examples is on the order of 3.9 and that of the latter is about 3.0, these insulating films cannot be used as interlayer insulating films which satisfies the condition $\epsilon \leq 2.0$ required for improvem nt of operating speed.

Besides the above, there is known a wiring technique called aerial wiring. In this technique, wiring is formed in the air without insertion of such an interlayer insulating film between metallic wirings. Although this aerial wiring technique makes it possible to attain approximately the condition of $\epsilon = 1.0$, the technique has a drawback in that the wiring metal tends to generate sagging and deformation because of the insufficient supporting portions of the wiring, which causes short-circuiting between the wirings and breaking of the wirings, giving rise the wirings with poor reliability.

SUMMARY OF THE INVENTION

It is, therefore, an object of the present invention to provide a semiconductor device which as a multilayered wiring structure with a small parasitic capacitance.

The semiconductor device in accordance with the present invention includes a semiconductor substrate on which are formed semiconductor elements, and a plurality of metallic wirings formed on the semiconductor substrate, the metallic wirings being formed in a multilayered form with porous insulating films interposed between adjacent wiring layers. Preferably, a porous insulating film is inserted between the metallic wirings as the interlayer insulating material, with the metallic wirings covered with a compact insulating film.

The diameter of the pores of the porous insulating film is preferable to be in the range of 5 to 50 nm, and the volumetric density of the pores of the porous insulating film is preferable to be in the range of 50 to 80 %.

Further, the forming process of the porous insulating film preferably includes the steps in which an insulating film which is a mixture of a basic oxide and an acidic oxide is deposited, then only the basic oxide or the acidic oxide is precipitated by a heat treatment, following that, only the basic oxide or the acidic oxide that is precipitated is dissolved. Pores are formed in the portions from which the above-mentioned substance is dissolved.

It is preferable to form the mixed insulating film as a mixture of sodium oxide or calcium oxide and silicon dioxide or silicon dioxide/boron oxide, and it is preferable to have the concentration of sodium oxide or calcium oxide contained in the mixed insulating film to be in the range of 15 to 25 mol %. After preparing the mixture as in the above, sodium oxide or calcium oxide along is dissolved. In the process of subjecting the mixed insulating

film to a h at treatment, it is preferable to set a temperature of the heat treatment in the range of 350 to 500° C.

In the present invention, a porous insulator having a large number of minute pores in an insulating film is used an an interlayer insulating film between the metallic wirings so that it is possible not only to reduce the relative dielectric constant of the interlayer insulating film (to less than or equal to 2) and but also to provide a metallic wiring sttucture with high reliability.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and further objects, features and advantages of the present invention will become more apparent from the following detailed description taken in conjunction with the accompanying drawings, wherein

Fig. 1 is a longitudinal cross-sectional view of the semiconductor device of a first embodiment of the present invention;

Fig. 2 is a longitudinal cross-sectional view of the semiconductor device of a second embodiment of the present invention;

Fig. 3 through Fig. 8 are longitudinal cross-sectional views for explaining a method of manufacturing the semiconductor device of the first embodiment of the present invention; and

Fig. 9 through Fig. 17 are longitudinal cross-sectional views for explaining a method of manufacturing the semiconductor device of the second embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

(First Embodiment)

As shown in Fig. 1, on a surface of a semiconductor substrate 101 having semiconductor elements formed thereon, these is formed an lonorgamic insulating layer 102 such as silicon oxide film, silicon nitride film or silicon oxynitride film as a passivation film. After forming contact holes in the insulating film 102, a first metallic wiring 103 is formed using pure aluminum, aluminum containing silicon or the like, and a porous insulating film 104 is deposited covering the first metallic wiring 103. Here, the porous insulating film 104 consists of an acidic oxide such as SiO_2, a basic inorganic insulator such as CaO or Li_2O or an organic insulator such as polyimide with volume density of pores of 50 - 80 %.

Then, after forming a metal 105 in the contact hole by electroless plating or low temperature CVD process, a second metallic wiring 106 is formed using a method similar to that of the first metallic wiring 103. Further, a porous insulating film 104 and a third metallic wiring 107 are formed using means similar to the above, and a metal 105, a fourth metallic wiring 108 and a topmost porous insulating film 104 covering the metallic wiring 108 are formed respectively.

Next, the method of manufacturing the semiconductor device shown in Fig. 1 will further be described in detail. First, as shown in Fig. 3, on the surface of a semiconductor substrate 301 having semiconductor elements formed thereon, there is deposited an inorganic insulating film 302 with two-layer structure of a silicon oxide film and a silicon oxynitride film. Here, the silicon oxide film is formed to have a thickness of about 1000 Å by a CVD method while the silicon oxynitride film is formed to have a thickness of about 3000 Å by a plasma CVD method.

Subsequently, after forming a contact hole 303 using a dry etching method, a first metallic wiring 304 is formed as shown in Fig. 4. The metallic wiring 304 is formed by deposition of pure aluminum metal by sputtering followed by a fine working using dry etching.

Then, a mixed insulating film 305 consisting of sodium oxide (Na_2O) and silicon oxide (SiO_2) is formed to have a thickness of 5000 Å as shown in Fig. 5. The mixed insulating film 305 is deposited by a CVD method, a coating method or a sputtering method so that the concentration of sodium oxide is in the range of 15 to 25 mol %. As the coating agent, use is made of a mixture of $R_1Si(OR_2)_3$ or $Si(OR_2)_4$ and NaOH with methyl-cellosolve used as the solvent. In the above, R_1 and R_2 represent hydrocarbon compounds of the form C_mH_n. In the case of formation of the film using the CVD method, deposition is carried out in reaction furnace by mixing SiH_4, N_2O, NaOH gases or organic silane series gases.

A multilayered wiring is formed by using thus formed mixed insulating films 305 as the interlayer insulating films. The case of building a four-layered metallic wiring is shown as an example in Fig. 6.

After forming a top layer of mixed insulating film as shown in Fig. 7, the mixed insulating film 305 is converted to a porous insulating film 306 as indicated in Fig. 8.

The conversion is carried out as in the following. A semiconductor substrate in the state of Fig. 7 is subjected to a heat treatment at a temperature in the range of 300 to 500 °C in an inert gas such

as nitrogen or an oxidizing atmosphere. As a result of such heat treatment, a phase separation phenomenon in which the mixed insulating film 305 is separated into Na_2O and SiO_2 takes place, giving rise to a micro-phase separation of "intertwining type" or "droplet type".

Then, by immersing the substrate in an acidic treatment solution such as hydrochloric acid, Na_2O alone is dissolved and there are formed holes in the portions from which Na_2O is dissolved out. The size of these pores depends upon that of Na_2O precipitation at the time of micro-phase separation. Under the conditions of heat treatment described above, there are formed numerous pores with diameter of about 10 nm.

In the above, the case of using the Na_2O/SiO_2 system which gives rise to a phase separation phenomenon as the mixed insulating film was described. However, similar effect can be obtained by employing other mixed insulating films of a basic oxide-an acidic oxide system which give rise to the phase separation phenomenon such as Li_2O/SiO_2 system and CaO/SiO_2 system.

Further, in the above embodiment, description was made in the case of carrying out the phase separation of the mixed insulating film 305 by the heat treatment in the last step. However, microphase separation may be introduced in each formation step of the mixed insulating film by providing heat treatment. It should be noted, however, that the dissolution of the precipitated insulator is to be carried out in the final step.

(Second Embodiment)

Referring to Fig. 2, the use of a porous insulating film 205 to be inserted between metallic wirings is analogous to the first embodiment, but a protective insulating film 204 is formed covering the surface of the wiring metals. The protective insulating film 204 is constructed by a compact film with passivation effect such as a silicon oxynitride film of thickness of 100 -2000 Å or a silicon nitride film with small stress.

The remaining constitution of the embodiment is the same as that of the first embodiment. Namely, on a semiconductor substrate 201 having semiconductor elements thereon, there is formed an inorganic insulating film 202 with a contact hole to separate the semiconductor substrate 201 from multilayered wiring layers to be laminated on it. Then, metal wiring 203 laminated in the form of a multilayer and porous insulating films 205 serving as interlayer insulating films are formed.

In the case of the present embodiment, wiring reliability can be improved to a large extent by isolating the porous insulating film 205 from the metallic wiring 203 by means of a protective insulating film 204.

Next, the method of manufacturing the semiconductor device shown in Fig. 2 will be described in detail. First, an inorganic insulating film 402 is deposited on the surface of a semiconductor 401 and then a contact hole 403 is formed as shown in Fig. 9.

Next, a first metallic wiring 404 is formed as shown in Fig. 10. Up to this step, things are the same as in the first embodiment.

Then, after forming a polyimide film 405 having a thickness of 5000 Å as an interlayer insulating film as shown in Fig. 11, a second metal wiring is formed on the polyimide film 405 as shown in Fig. 12. The case of a multilayered wirings of four layers is illustrated as an example in Fig. 13.

Next, the polyimide films 405 used as the interlayer insulating films are removed completely by an O_2 plasma treatment as shown in Fig. 14. Then, a protective insulating film 406 is formed using a compact substance such as silicon nitride to cover the metal wiring 404 as shown in Fig. 15. The protective insulating film 406 is deposited by a plasma CVD method to have a thickness in the range of 500 to 1000 Å.

Next, as shown in Fig. 16, after forming a mixed insulating film 407 using a mixed insulator of a basic oxide/an acidic oxide which is microphase separable by heat treatment as described in the first embodiment, the mixed insulating films 407 are converted to porous insulating films as shown in Fig. 17.

In this embodiment, the metal wirings are coated with a protective insulator so that there is obtained an effect of improving the reliability of the wirings compared with the first embodiment.

In the foregoing, the first embodiment as well as the second embodiment are described, but it is possible to realize a variety of alterations and additions. For example, pores can be formed easily by mixing in advance 50 mol % or less of alkyl groups such as CH_3, C_2H_5, C_3H_7 in a basic oxide or an acidic oxide, and then removing the alkyl group by subjecting the product to a heat treatment of 300 - 500 °C. The heat treatment in this case will become effective by carrying it out in a vacuum of equal to or smaller than 10 Torr in an atmosphere with a trace of nitrogen or oxygen. Moreover, the reliability of the wirings can be enhanced, for example, by adding a step of removing impurities that are sticking to the side walls of the pores by giving a baking after formation of the porous insulating films, by forming an overall passivation film after formation of a multilayered wiring according to the present methods, and the like.

Claims

1. A semiconductor device comprising:
a semiconductor substrate having semiconductor elements formed ther on;
a plurality of wiring layers formed in a multilayered form on said semiconductor substrate to interconnect said semiconductor elements; and
porous insulating films interposed between adjacent layers of said wiring layers.

2. A semiconductor device as claimed in claim 1, further comprising a compact insulating film formed on the surface of said wiring layers.

3. A semiconductor device as claimed in claim 1, wherein the diameter of the pores of said porous insulating film is in the range of from 5 nm to 50 nm.

4. A semiconductor device as claimed in claim 2, wherein the diameter of the pores of said porous insulating film is in the range of from 5 nm to 50 nm.

5. A semiconductor device as claimed in claim 1, wherein the volume of the pores in said porous insulating film is in the range of from 50% to 80% of the volume of said porous insulating film.

6. A semiconductor device as claimed in claim 2, wherein the volume of the pores in said porous insulating film is in the range of from 50% to 80% of the volume of said porous insulating film.

7. A semiconductor device as claimed in claim 5, wherein said porous insulating film is made of a material selected from the group of acidic oxides such as SiO_2, basic inorganic insulators such as CaO, Na_2O and Li_2O, and organic insulators such as polyimide.

8. A semiconductor device as claimed in claim 6, wherein said porous insulating film is made of a material selected from the group of acidic oxided such as SiO_2, basic inorganic insulators such as CaO, Na_2O and Li_2O, and organic insulators such as polyimide.

9. A semiconductor device as claimed in claim 2, wherein said compact insulating film is made of silicon oxynitride film or silicon nitride film.

10. A semiconductor device comprising:
a semiconductor substrate having semiconductor elements formed thereon;
a plurality of wiring layers formed in a multilayered form on said semiconductor substrate via porous insulating films; and
a compact insulating film formed on the surface of the wiring layers covering them.

11. A semiconductor device comprising:
a semiconductor substrate having semiconductor elements formed thereon;
a porous insulating film formed on said semiconductor substrate; and
a wiring layer formed on said porous insulating film.

12. A method of manufacturing semiconductor device comprising the steps of:
depositing an insulating film which is a mixture of a basic oxide and an acidic oxide on a semiconductor substrate having semiconductor elements formed thereon;
subjecting said mixed insulating film to a heat-treatment;
forming a porous insulating film by selectively removing said basic oxide or said acidic oxide; and
forming a wiring layer on said porous insulating film.

13. A method of manufacturing semiconductor device comprising the steps of:
forming a multilayered wirings using an organic substance as an interlayer insulating film;
removing said organic substance;
forming a compact insulating film covering the surface of said multilayered wirings;
forming next an insulating film which is a mixture of a basic oxide and an acidic oxide between said multilayered wirings;
subjecting said mixed insulating film to a heat treatment; and
forming a porous insulating film by selectively removing said basic oxide or said acidic oxide.

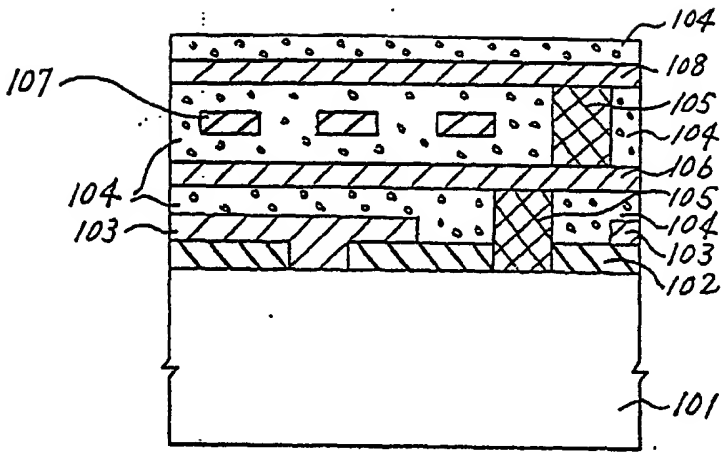
104
108
107
105
104
106
104
105
104
103
103
102
101

Fig. 1

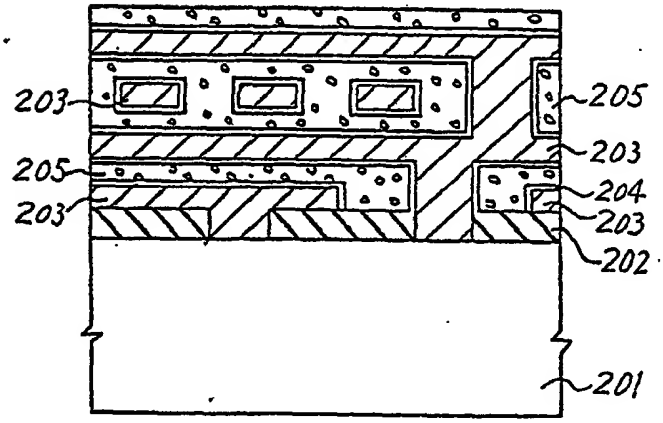
203
205
205
203
203
204
203
202
201

Fig. 2

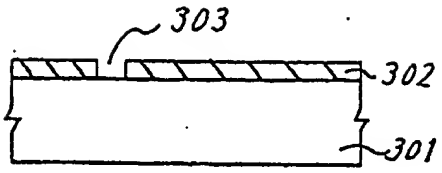

Fig. 3

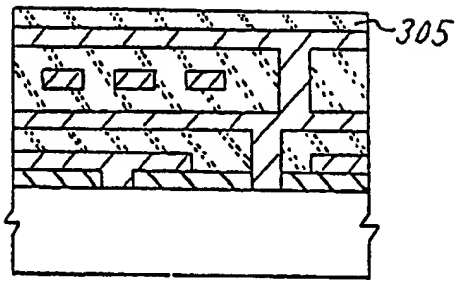

Fig. 7

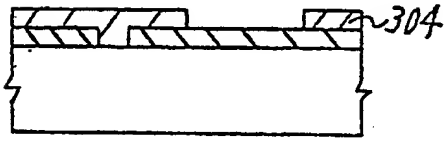

Fig. 4

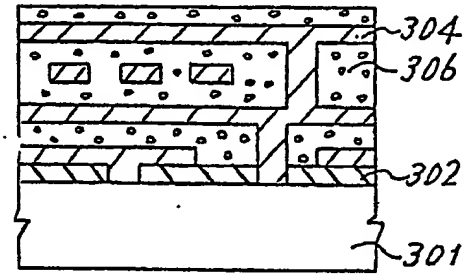

Fig. 8

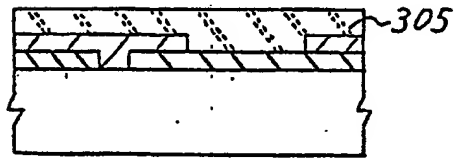

Fig. 5

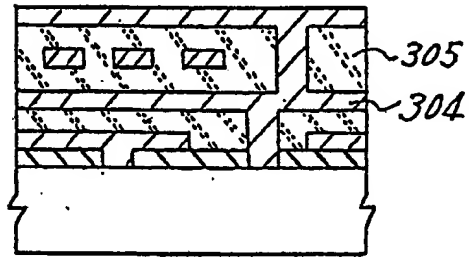

Fig. 6

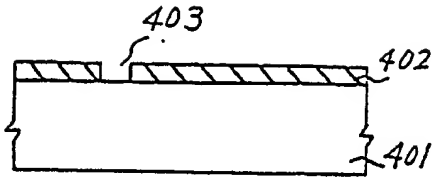

Fig. 9

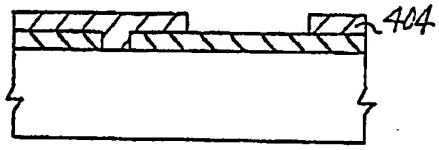

Fig. 10

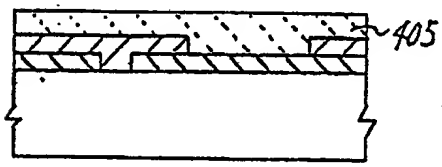

Fig. 11

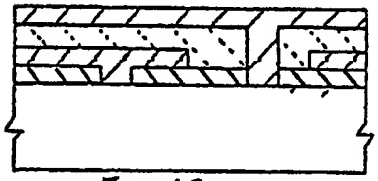

Fig. 12

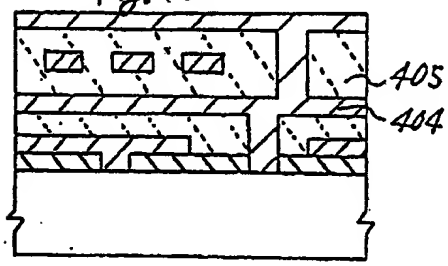

Fig. 13

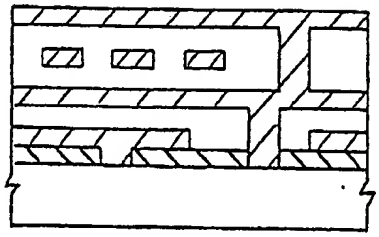

Fig. 14

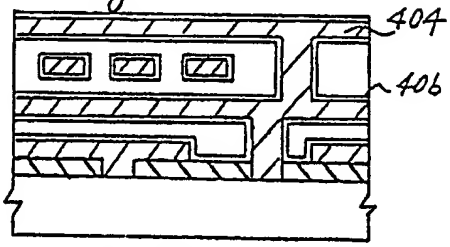

Fig. 15

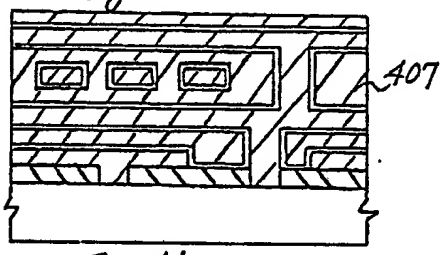

Fig. 16

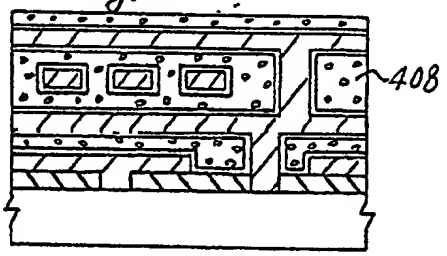

Fig. 17